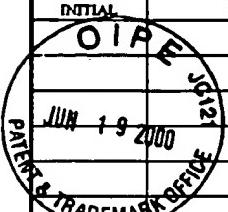


FACSIMILE OF FORM PTO-1449 (REV. 6-89)		U.S. DEPARTMENT OF COMMERCE Patent and Trademark Office		ATTORNEY'S DOCKET NUMBER <b>98RSS367</b>		SERIAL NUMBER <b>09/557,454</b>	
<b>INFORMATION DISCLOSURE CITATION</b> (Use Several Sheets if Necessary)				APPLICANTS <b>Lester J. Kozlowski et al.</b>		<b>RECEIVED</b>	
				FILING DATE <b>April 24, 2000</b>	GROUP ART UNIT		JUL 26 2000
<b>Group 2700</b>							
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
							
<b>FOREIGN PATENT DOCUMENTS</b>							
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES      NO	
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)							
KJ	AA	CMOS: Circuit Design, Layout, and Simulation; R. Jacob Baker, Harry W. Li and David E. Boyce, 1998, Chpt. 2-4.					
KJ	BB	Integrated Circuit Manufacturability, The Art of Process and Design Integration, Dhiraj K. Pradhan, 1999, Chpt. 4-5.					
EXAMINER		<i>Kelly J. Q.</i>			DATE CONSIDERED <b>9/9/05</b>		
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.							